VMEC EQUIPMENT/SEED GRANT RESEARCH SUMMARY

PROPOSAL TITLE:

Ultralow-power straintronic switch implemented with a nanomagnet and a topological insulator for "processor in memory" architectures

RESEARCH SUMMARY:

Processor-In-Memory (PiM) architectures are designed to circumvent the present day "Von Neumann bottleneck" in conventional silicon computing. This bottleneck arises from the physical separation of processor and memory cores, and the resulting delay in data transfer between the two. The data transfer link is also wasteful of energy and a target for cyberattacks. PiM architectures circumvent this shortcoming by carrying out processing within the memory core, thereby eliminating the need for the link.

We propose to lay the groundwork for a new PiM architecture proposed by one of the PIs (AG) [1], involving emerging materials and their novel underlying physics. The critical element of this architecture is a novel switch that exploits the reciprocal interaction between a ferromagnetic (FM) film grown on a 3-D topological insulator (TI) film whose bulk is insulating but surface states are conducting. The FM layer is designed to have perpendicular magnetic anisotropy, which makes the magnetization point out of the magnet's plane. By applying a strain to the FM using a piezoelectric layer, the magnetization can be moved from out- to in-plane, which will close an energy gap in the TI's surface states and increase the surface current, thereby switching the device from OFF to ON. Such a device can act as a row-column selector. The random addressed TI-FM cell can then be enabled to write information onto a magnetic storage element, subsequent to which, one can use a sense amplifier to execute key Boolean logic gate operations directly and in parallel on entire rows of locally stored data. This VMEC proposal will establish the computational infrastructure for studying the performance metrics of this device, which will also be fabricated and characterized to demonstrate the out-of-plane to in-plane switching of the magnet's magnetization due to strain, and ensuing modulation of the TI-FM heterostructure's overall conductance. Since it could take only a few tens mV to generate the strain required to switch, the switching action will be extremely energy efficient (few aJ expended to switch). and take place in less than 1 ns, which promises a clock rate of ~GHz.

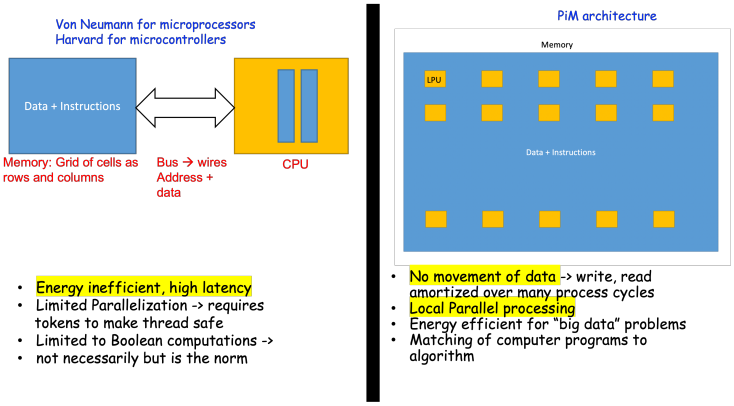

Fig. 1: Comparison between von-Neumann and PiM architectures

Research Background: The memory hierarchy. Conventional Von Neumann architecture has separate memory and logic elements with data buses connecting the two. Since memory scales slower than logic, this creates a 'memory wall' (weaknesses summarized in Fig. 1). In contrast, a PiM architecture involves no data movement between logic and memory cores, and relies on local parallel processing of data. Designing an

energy-efficient, ultra-scaled PiM architecture is challenging, but brings significant dividends.

2: FM/TI hybrids: The proposed device is an FM/TI heterostructure to enable an extremely energy-efficient row/column selector in PiM architecture**.**

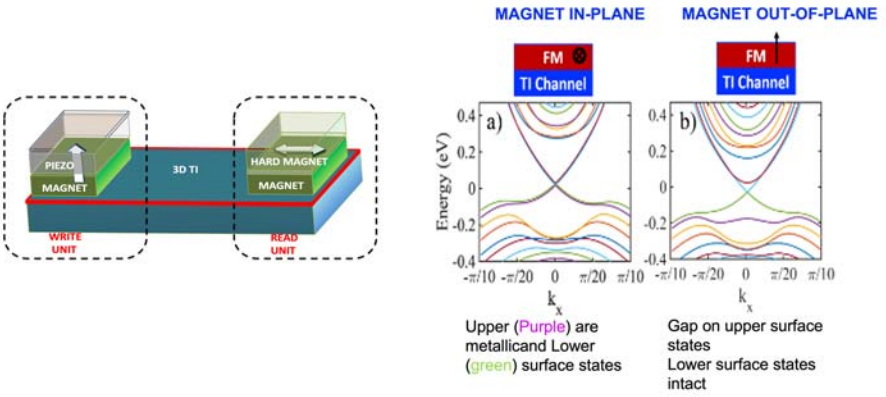

Fig. 2: (left panel) One possible rendition of the device where the piezoelectric layer for generating strain is placed on top of the magnet; (b) Calculated band structure of surface states of the TI when the magnetization of the magnet is in-plane and out-of-plane

The PI's group had repeatedly demonstrated that the magnetization of a magnetostrictive nanomagnet elastically coupled to an underlying piezoelectric substrate can be switched very efficiently by applying electrically generated mechanical strain [2]. When strain is applied to a magnetostrictive thin film with perpendicular magnetic anisotropy, it will rotate the magnetization by 90 degrees and bring it from out-of-plane to in-plane. This realizes the switching action in the proposed device shown in Fig. 2. The electrically generated strain acts like gate control to switch the conductance. Note that this is an enhancement mode (normally off) switch. With it, one can build a 1-bit FM-TI-FM memory cell which can be individually addressed with a row and column selector in a crossbar array.

We can thus read multiple rows on shared read lines and use a sense amplifier whose threshold can be modified as per the logic operation (e.g., 0.5 times the row current for a 2 word OR gate, 1.5 times for a 2 word AND). This leads to the PiM architecture proposed by co-PI Avik Ghosh.

Proposed Research Task 1: (lead Ghosh): One of our preliminary results is that while the TI has a small ~200 meV bandgap, that is sufficient to get high accuracy write for FM/TI based cache memory. An initial estimate based on 3-D atomistic tight binding models for TIs posits that current leakage into the small bandgap as well as along the sides of the TI slab do not severely compromise the reliability, as the downstream FM can only be activated when the local spin current exceeds a threshold set by material properties. This proposal will extend this estimate with a full-scale atomistic Density Functional Theory for the material modeling, then couple with full quantum kinetics to capture spin orbit torque and the accumulation of spin using the Rashba-Edelstein effect from the spin-momentum locked topological surface states. These will then be translated to SPICE compatible models and subsequently used to study the full PiM (selector-write-read-sensor) stack. We will explore various magnetic and TI materials for material optimization and work to refine the experimental design.

Proposed Research Task 2 (lead Bandyopadhyay): Bandyopadhyay will be in charge of device fabrication and measurements. He will be provided with a heterostructure comprising a piezoelectric layer grown on top of an ultrathin magnetic layer which is grown on top of a TI thin film. This structure will be provided by a collaborator at no charge. His tasks are:

1: Fabrication of the device using reactive ion etching. The electrical contacts will be delineated with optical lithography for relatively large structures and e-beam lithography for small structures. The electrode materials will be Al or Au. All processing steps will be carried out in the Virginia Microelectronics Center cleanroom at VCU.
2: The switching action will be demonstrated by measuring the transfer characteristics of the device (current flowing between the source and drain contacts in Fig. 3 as a function of the gate voltage). The gate voltage generates strain in the piezoelectric layer which rotates the magnetization of the magnetic layer from out of plane to in-plane and closes the energy gap in the TI, thereby increasing the source to drain current. These measurements will be made using a Semiconductor Parameter Analyzer at VCU. The obtained characteristics will yield measurement of the current ON/OFF ratio for maximum strain and also the device transconductance.

Expenses : The funding will be utilized to pay the annual stipend of a graduate student at VCU who will carry out all fabrication and measurements. An amount of $5 K has been budgeted for material cost and lab charges. Computational cost has been budgeted at $12 K.

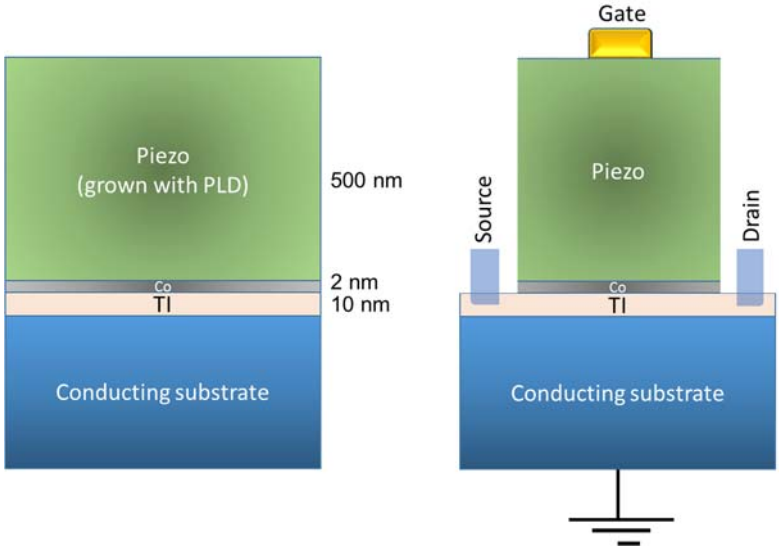

Fig. 3: Schematic of the structure to be fabricated.

Impact on the Commonwealth : There are numerous industries in the State of Virginia that can benefit from the research proposed here. That includes VMEC members like BAE Systems and Micron, who are heavily involved with silicon platforms for computing and information processing. As Virginia poises herself to play a major role in semiconductors buoyed by the CHIPS act established by the Congress and the Senate, novel devices and architectures will garner increasing attention. The PiM architecture discussed here leads to several advances – increased energy efficiency, better resilience against cyberattacks and high speed computing. There is a drive to move data processing out of the cloud into the edge for internet of things and this research is synergistic with this vision. Two premier research universities in Virginia, with strong programs in semiconductor devices, are collaborating in this proposal to innovate a new device that can lead to disruptive technologies. Additionally, we expect to involve undergraduate students working on capstone projects in some elements of this research. These trained students will constitute a valuable pool of skilled workers in the State of Virginia.

References :

1. H. Vakili, et al., www.arXiv.org, article 2203.14389 (2022)
2. N. D'Souza, et al., Nano Letters, 16, 1069-1075 (2016).